Nishant Bakshi

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Analog/mixed-signal design engineer with an MSEE from USC and 2+ years in semiconductor reliability and test engineering. Hands on experience spanning transistor-level CMOS design, silicon bring-up and characterization, and mixed-signal PCB design.

Technical Skills

Design & Simulation: Cadence Spectre, LTSpice, PySpice, PLECS
Layout & PCB: Cadence Virtuoso, Altium Designer, KiCAD
Programming: Python, C/C++, JSL (JMP), LabVIEW, Git
Test & Characterization: Probe Station, Parametric Analyzer, Curve Tracer
Reliability: TDDB, NBTI, HCI, Vramp, JESD47, AEC-Q100

Experience

Product & System Designer Jan. 2026 – Present
Common Wave Hi-Fi *Los Angeles, CA*

- Designed 3 loudspeaker and crossover systems using BEM/LPM simulation, validated by gated acoustic measurement
- Built a custom impedance-analysis test fixture; repaired 20+ vintage tube and transistor amplifiers at component level

Graduate Research Assistant May 2025 – May 2026
IEDM Group, University of Southern California *Los Angeles, CA*

- Diagnosed and characterized a custom 64-channel, 640MHz sample-and-hold CMOS chip
- Contributing to a publication in *IEEE Solid-State Circuits Letters*
- Designed a test PCB and wire-bonding diagram for the custom chip; interfaced with packaging vendors for assembly
- Assembled, reworked, and brought up mixed-signal PCBs for silicon validation, including SMD soldering
- Designed and simulated a 15MHz programmable transimpedance amplifier for a board-level neuromorphic RF classifier

Engineer II – Device Sep. 2022 – Aug. 2024
Microchip Technology Inc. *Colorado Springs, CO*

- Developed C++/Python/LabVIEW stress-test programs for TDDB, NBTI, HCI, and Vramp reliability testing
- Authored 3 reliability reports for 180nm+ CMOS technologies, supporting JESD47 and AEC-Q100 qualifications.
- Characterized L-dependent Pelgrom mismatch on halo-implanted CMOS technology across 6,500+ MOSFETs
- Built data-analysis scripts in JMP that replaced manual Excel workflows, cutting reporting time from 2 weeks to 2–4 days
- Identified inconsistent qualification methodology across 5 internal labs and drove changes to bring testing back into alignment

Projects

250W Two-Switch Forward Converter | *PLECS, Magnetics Design* Apr. – May 2026

- Designed a 450V-to-190V converter with custom transformer and inductor magnetics, and a Type-II compensator
- Simulated 92.6% efficiency at 300W with sub-2% output ripple under load transients

12-Bit 10MS/s Asynchronous SAR ADC | *TSMC 45nm, Cadence Spectre* Mar. – May 2025

- Designed the differential CDAC, StrongARM comparator, and self-timed asynchronous control logic
- Applied monotonic switching and bottom-plate sampling to reduce pedestal error and eliminate static power
- Achieved 9.03-bit ENOB (56.1 dB SNDR) at 1MHz, with waveforms recovered via a custom Python post-processing script

180nm 5.7GHz Rail-to-Rail OTA | *Cadence Virtuoso/Spectre* Oct. – Dec. 2024

- Designed a rail-to-rail folded-cascode OTA achieving 51 dB DC gain, 5.7 GHz unity-gain bandwidth
- Implemented a differential-difference amplifier feedback circuit to set DC output voltage level without poly resistor

Education

University of Southern California Aug. 2024 – May 2026
M.S. Electrical Engineering *Los Angeles, CA*

New York University Aug. 2018 – May 2022
B.S. Electrical Engineering *New York, NY*

Publication

- M. Hamada, M. Toubar, Z. Wang, **N. Bakshi**, H.-C. Chen, M. Palaria, J. Yang, and M. S.-W. Chen, "A 1.2-V, 8.5-ns Settling, Bi-Slewing CMOS Driver for Heavy Loads in Discrete-Time Analog Computing Applications," *IEEE Solid-State Circuits Letters*, in press.